CLAIM AMENDMENTS

1. (Currently Amended) A half-rate clock and data recovery (CDR) circuit including a half-rate phase detector for detecting phases of an input signal and a half-rate clock, a charge pump circuit, a low-pass filter, and a voltage controlled oscillator for feeding the half-rate clock back to the half-rate phase detector, the half-rate phase detector comprising:

first-stage and second-stage latch circuits;

~~further~~ additional first-stage and second-stage latch circuits;

a selector circuit which receives an output of the first-stage latch circuit and an output of the ~~further~~ additional first-stage latch circuit ~~so as to output~~ and outputs a ~~retimed~~ re-timed signal in response;

a first exclusive OR circuit which receives an output of the second-stage latch circuit and an output of the ~~further~~ additional second-stage latch circuit ~~so as to output~~ outputs a reference signal in response;

a latch delay circuit ~~which is provided on~~ in a through-data path;

a one-pulse delay circuit ~~which is provided on~~ in the through-data path ~~so as to receive~~ and receiving an output of the latch delay circuit and ~~outputs~~ outputting through-data for generating a delay ~~amount~~ of one pulse; and

a second exclusive OR circuit which receives the ~~retimed~~ re-timed signal from the selector circuit and the through-data from the one-pulse delay circuit ~~so as to output~~ and outputs an output signal~~;~~ in response, wherein the voltage controlled oscillator is an N type LC voltage controlled oscillator because of phase comparison polarity of the half-rate phase detector ~~provided with~~ including the one-pulse delay circuit ~~enables use of an N type LC voltage controlled oscillator as the voltage controlled oscillator~~.

2. (Currently Amended) The half-rate CDR circuit according to Claim 1, wherein ~~a~~ gate size of the one-pulse delay circuit of the half-rate phase detector is variable ~~such that fine~~ for adjustment of the delay ~~amount~~ of one pulse in the one-pulse delay circuit ~~can be performed~~.

3. (Currently Amended) The half-rate CDR circuit according to Claim 1, wherein ~~a~~ wiring length of the one-pulse delay circuit of the half-rate phase detector is variable ~~such that fine~~ for adjustment of the delay ~~amount~~ of one pulse in the one-pulse delay circuit ~~can be performed~~.

4. (Currently Amended) The half-rate CDR circuit according to Claim 1, ~~wherein~~ including a plurality of pump-up bias circuits having different gate bias levels, respectively ~~are provided,~~ for a pump-up constant current source of the charge pump circuit and ~~a~~ for changing current quantity of the pump-up constant current source ~~is changed~~ upon ~~changeover~~ switching of the pump-up bias circuits ~~such that fine,~~ for adjustment of the delay ~~amount~~ of one pulse in the one-pulse delay circuit ~~can be performed~~.

5. (Currently Amended) The half-rate CDR circuit according to Claim 1, ~~wherein~~ including a plurality of pump-down bias circuits having different gate bias levels, respectively ~~are provided,~~ for a pump-down constant current source of the charge pump circuit and ~~a~~ for changing current quantity of the pump-down constant current source ~~is changed~~ upon ~~changeover~~ switching of the pump-up bias circuits ~~such that fine,~~ for adjustment of the delay ~~amount~~ of one pulse in the one-pulse delay circuit ~~can be performed~~.

6. (Currently Amended) The half-rate CDR circuit according to Claim ~~1~~ 4, wherein the number of pump-up constant current sources of the charge pump circuit is changed ~~so as~~ to change ~~a~~ the current quantity of the pump-up constant current sources ~~such that fine~~ for adjustment of the delay ~~amount~~ of one pulse in the one-pulse delay circuit ~~can be performed~~.

7. (Currently Amended) The half-rate CDR circuit according to Claim ~~1~~ 5, wherein the number of pump-down constant current sources of the charge pump circuit is changed ~~so as~~ to change ~~a~~ the current quantity of the pump-down constant current sources ~~such that fine~~ for adjustment of the delay ~~amount~~ of one pulse in the one-pulse delay circuit ~~can be performed~~.